Contents

2 Detailed Design

2.1 Module Description

The Management Module provides the manage interface to the client. Client can configure MAC and PHY via this interface. Besides, statistic information is provided too. Figure 2-1 shows a block diagram of Management Module, with

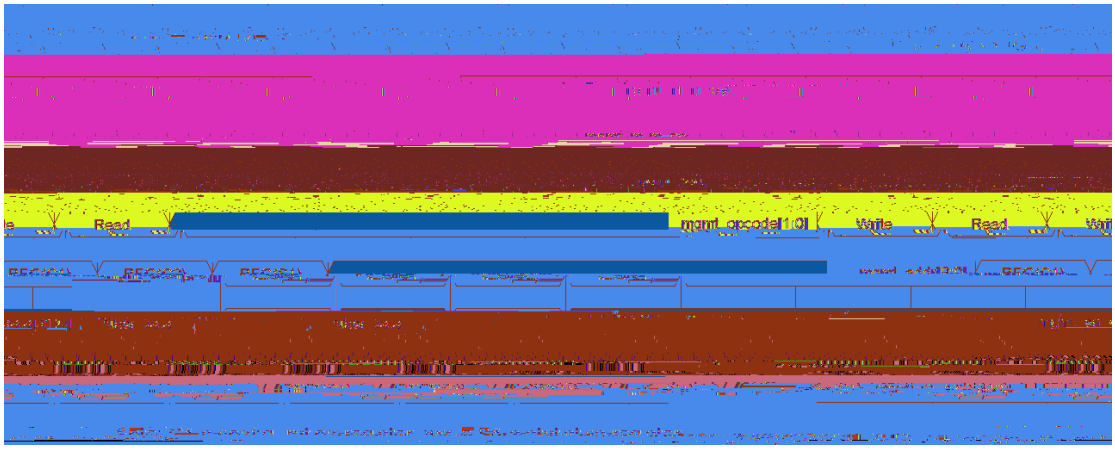

Figure 2-2 Internal Register Operating Timing

Operating Timing of Internal registers (configuration and statistics registers) is shown in Figure 2-2. New value written to internal registers will be valid one clock after the write request. The written value will appear on mgmt_rd_data two cycles after the write request, which is the same as read operation. Statistics registers are 64bit width, so its reading process will take 2 clocks.

T/T2 1 Tf12 0 0 12 89.88 570.260304.46 Tc0 Tw()w[[ock aWhe waake60.,wh]Tjsamsen6.

Port Name	Direction	Description

Table 2-5 lists the I/Os that interface from Transmit Engine.

Bit	Description
31:0	Lower 32bit of MAC Address

Table 2-8 Receiver Configuration Word 0

Figure 2-7 block diagram of Management Register Sub-module

MDIO

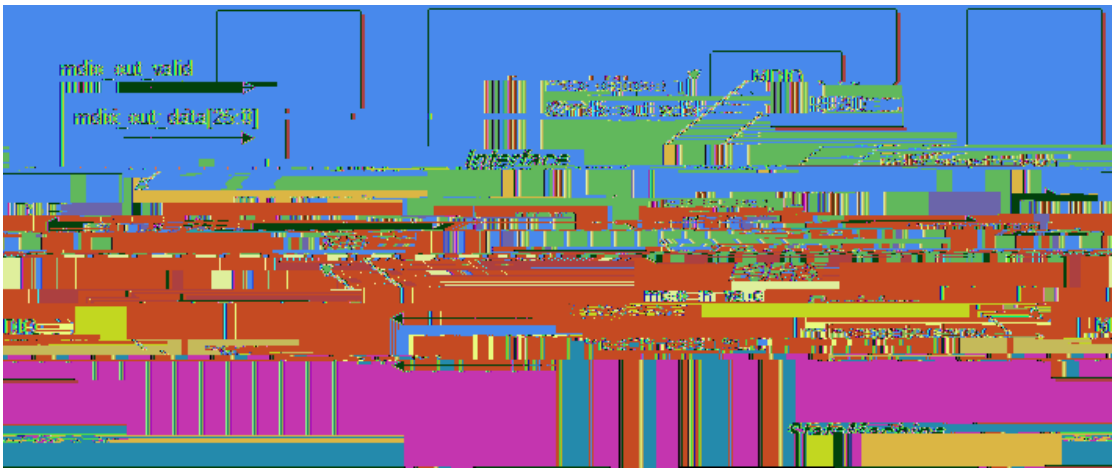

Figure 2-8 block diagram of MDIO Sub-module

2.5 Code Listing

Source Code Name	Version	Date