# Revision History

| Date | Author | [redacted] | [redacted] |
| --- | --- | --- | --- |

# Reference

[1] 10G Ethernet Mac System Design Issue 1.0
[2] Xilinx LogiCORE 10-Gigabit Ethernet MAC User Guide
[3] IEEE 802.3ae Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation

# 2 Detailed Design

| | | |
|---|---|---|
| tx_ack | Output | Output Handshaking signal. Asserted when the first column of data on TX_DATA has been accepted |

## 2.3 Module Design

The transmit engine contains several blocks; input and output FIFO/register, control logic and counters. The input and output FIFO/registers are employ to receive data from the client and

The control logic is essentially a state machine that controls how the data is output to the physical by selecting between the control bytes and the client data. There are four different states in the control logic and there are IDLE, START, DATA and PAUSE.

In the IDLE state, IDLE bytes (07) are transmitted to the physical. When a receive fault occurs, the state machine will be stuck at IDLE until the signal is de-asserted.

In the START state, START control bytes, PREAMBLE bytes and Start Frame Delimiter are loaded into the output. Once the data is loaded, the state changed to DATA.

In the DATA state, the FIFO empty 64 bits at a time to the output until the empty flag is set. In this state, the tx_data_valid bytes are inverted and output to the command output, txc.
If the empty flag is asserted in any of the FIFO, the output register with no valid data will be loaded with the TERMINATE and IDLE control byte

## 2.5 Code Listing

Firmware

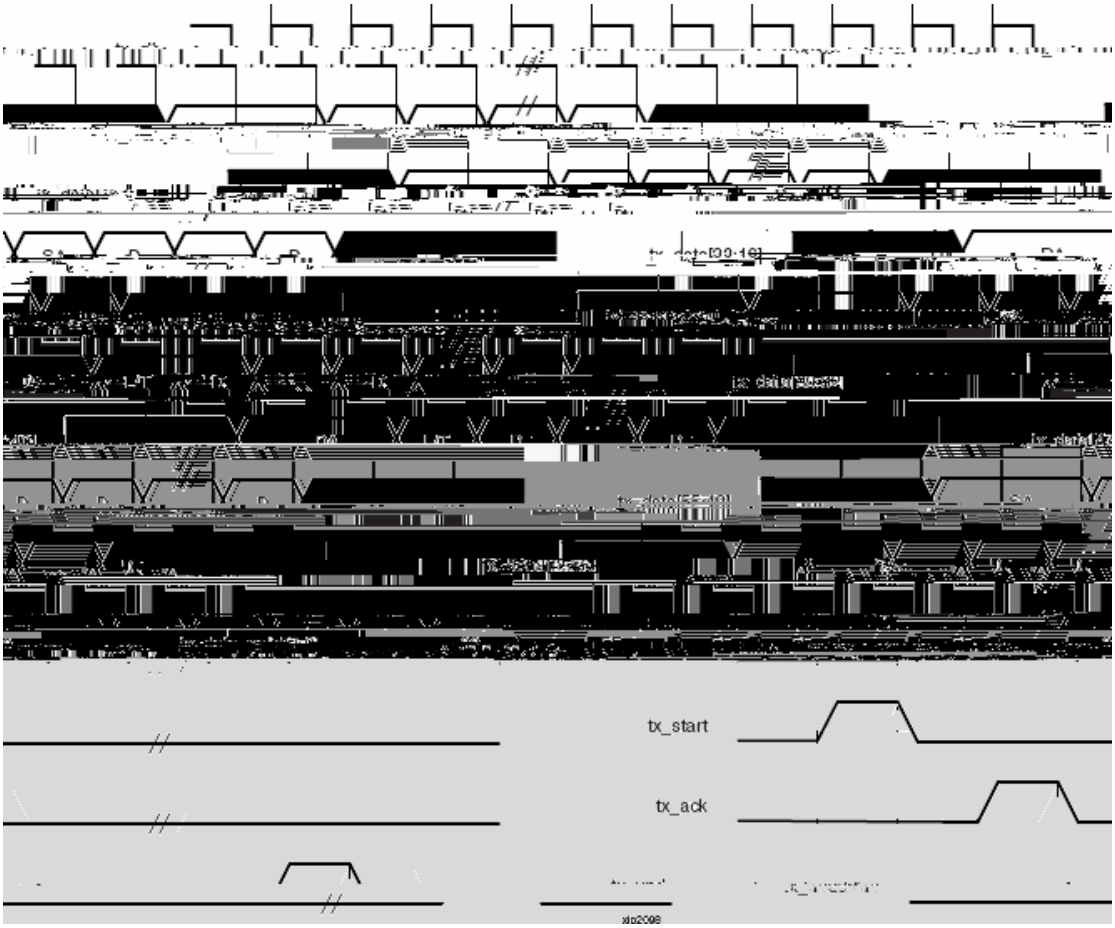
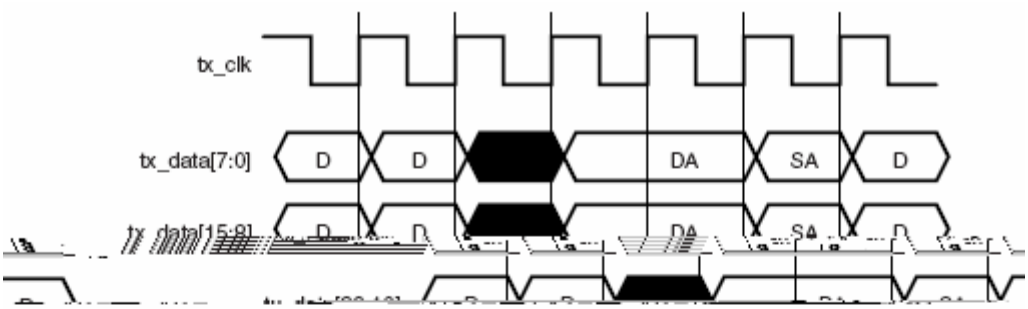



**Figure 0-3 Aborting a frame transmission [Ref. 2]**

Figure 2-5 shows the abortion of a frame by asserting the tx_underrun signal. The current frame is stopped from transmission. (What happen when is aborted, do I insert an error control character)


tx_clk
tx_data[7:0]
D
D
DA
SA
D