5x4Gbps 0.35 Micron CMOS CRC Generator Designed With Standard Cells

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Abstract

Design highlights for a 32-bit parallel and highly pipelined Cyclic Redundancy Code (CRC) generator are

and $Word$ is the input word (16 bits.) The ' ' sign denotes a multiplication modulo the polynomial within the Galois Field.

3. HARDWARE IMPLEMENTATION

The main problem is the Galois Field multiplier which is the subcircuit that implements the '$CRC(N) \quad \alpha^{16}$' operation. The so-called "H-matrix" (depicted in figure 1)