Revision History


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I²S sign

5.2.5 TxIntStat – Description

A bit in this register is set to 1 when an event occurs. If the corresponding bit in TxIntMask is set to 1, an interrupt is generated (if enabled). Write a 1 to a bit to clear the event. The interrupt signal goes inactive when all events have been cleared.

Bit #	Access	Name	Description
31-16	R	-	Unused
15-2	R	-	Unused
1	RW	HSBF	Higher sample buffer empty
0		LSBF	Lower sample buffer empty