1. Introduction

2.2. Technical Details

Below is a summary of main features of each CoreConnect bus.

2.2.1. PLB

- High Performance bus (Processor Local Bus)
- Overlapped read and write (up to two transfers per cycle)
- Split transfer support
- Address pipelining (reduces latency)
- Separate read and write data
- 32-64+ bit data bus with
- 32 bit address space
- support for 16-64 byte bursts
- supports byte enabling (0aa seigneand wr3yte enansfers p

- SeLe red wrhidden art ate ionureduces latency)

3. AMBA

5. The Last Word

As much as I wished to leave political motivation out of this report, I feel it is impossible in today world of patients and lawsuits. Both AMBA and CoreConnect are controlled by large, major corporations (ARM and IBM). Even though they claim that customer comments and suggestions are considered, the final decision of evvh thod to

6. References

ARM Corp, AMBA

http://www.arm.com/sitearchitek/armtech.ns4/html/amba?OpenDocument&style=SoC_Customization

IBM Corp, CoreConnect

http://www.chips.ibm.com/products/coreconnect/

Silicore Corp, WISHBONE

http://www.silicore.net/pdfiles/wishbone.pdf

Silicore Corp, press release, releasing WISHBONE to public domain

http://ww