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4.2 SIGNAL DESCRIPTION.....

Chapter 1 - Introduction

The WISHBONE[1] System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores is a flexible design methodology for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating System-on-Chip integration problems. This is accomplished by creating a

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formation. They are especially useful when novel or unusual control signals (such as parity, cache control or interrupt acknowledge) are needed on an interface.

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- **RULE**
- **RECOMMENDATION**
- **SUGGESTION**
- **PERMISSION**
- **OBSERVATION**

Any text not labeled with one of these keywords describes the operation in a narrative style. The keywords are defined as follows:

RULE
Rules form the basic framework of the specification. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules MUST be followed to ensure

RECOMMENDATION

1.4 Use of Timing Diagrams

Figure 1-1 shows some of the key features of the timing diagrams in this specification. Unless otherwise noted, the MASTER signal names are referenced in the timing diagrams. In some cases the MASTER and SLAVE signal names are different. For example, in the point-to-point interconnections the [ADR_O] and [ADR_I] signals are connected together. Furthermore, the actual waveforms at the SLAVE may vary from those at the MASTER. That's because the MASTER and SLAVE interfaces can be connected together in different ways. Unless otherwise noted, the timing diagrams refer to the connection diagram shown in Figure 1-2.

ASIC
Acronym for: Application Specific Integrated Circuit. A general term which describes a generic array of logic gates or analog building blocks which are programmed by a metalization layer at a silicon foundry. High level circuit descriptions are impressed upon the logic gates or analog building blocks in the form of metal in-0f.5(A)-6.4(c)ts.

The ordering of data during a transfer. Generally, 8-bit (byte) data can be stored with the most

Fixed Interconnection
An interconnection system that is fixed, and *cannot*

Hardware Description Language (HDL)
(1) Acronym for: Hardware Description Language. E

An off-chip interconnection is used when a WISHBONE interface extends off-chip. See Figure 1-6.

Figure 1-6. Off-chip interconnection.

Operand Size

The operand size is the largest single unit of data that is moved through an interface. For exam-

Figure 1-8. Shared bus interconnection.

Acronym for: Versa Module Eurocard bus. A popular microcomputer (board) bus. While this

1.8 References

IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition. IEEE Press 2000.

Chapter 2 – Interface Specification

This chapter describes the signaling method between the MASTER interface, SLAVE interface, and SYSCON module. This includes numerous options which may or may not be present on a particular interface. Furthermore, it describes a minimum level of required documentation that must be created for each IP core.

2.1 Required Documentation for IP Cores

WISHBONE compatible IP cores include documentation that describes the interface. This helps the end user understand the operation of the core, and how to connect it to other cores. This documentation takes the form of a WISHBONE DATASHEET. It can be included as part of the

(6) All interfaces that support tag signals MUST describe the name, TAG TYPE and operation of the tag in the WISHBONE DATASHEET.

(7) The WISHBONE DATASHEET MUST indicate the port size. The port size MUST be indicated as: 8-bit, 16-bit, 32-bit or 64-bit.

RECOMENDATION 2.00
It is recommended that the interface uses the signal names defined in this document.

CLK_O

The system clock output [CLK_O] is generated by the SYSCON module. It coordinates all activities for the internal logic within the WISHBONE interconnect. The INTERCON module connects the [CLK_O] output to the [CLK_I] input on MASTER and SLAVE interfaces.

RST_O

TERCON does not grant the bus to any other MASTER, until the current MASTER negates [LOCK_O] or [CYC_O].

RTY_I

The retry input [RTY_I] indicates that the interface is not ready to accept or send data, and that

RULE 3.00
All WISHBONE interfaces MUST initialize themselves at the rising [CLK_I] edge following the

PERMISSION 3.15
Other signals, besides [CYC_I] and [STB_I], MAY be included in the generation of the cycle termination signals.

OBSERVATION 3.30

OBSERVATION 3.40
The asynchronous assertion of [ACK_O], [ERR_O], and [RTY_O] assures that the interface can accomplish one data transfer per clock cycle. Furthermore, it simplifies the design of arbiters in multi-MASTER applications.

3.2.2 SINGLE WRITE Cycle

3.3 BLOCK READ / WRITE Cycles

The BLOCK transfer cycles perform multiple data transfers. They are very similar to single READ and WRITE cycles, but have a few special mod406 693.1 Nto siupportmultiple

3.3.1 BLOCK READ Cycle

SLAVE presents valid data on [DAT_I()] and [TGD_I()].
MASTER monitors [ACK_I], and prepares to latch [DAT_I()] and

Figure 3-6. BLOCK READ cycle.

Figure 3-7. BLOCK WRITE cycle.

MASTER presents new bank select [SEL_O()] to indicate where it sends data.
MASTER asserts [STB_O].

SETUP, EDGE 3: SLAVE decodes inputs, and responds by asserting [ACK_I].
SLAVE prepares to latch data on [DAT_O()] and [TGD_O()].
MASTER monitors [ACK_I], and prepares to terminate data phase.

Note: any number of wait states can be inserted by the SLAVE at this point.

Figure 3-8. RMW cycle.

3.5 Data Organization

Data organization refers to the ordering of data during transfers. There are two general types of ordering. These are called BIG ENDIAN and LITTLE ENDIAN. BIG ENDIAN refers to data ordering where the most significant portion of an operand is stored at the lower address. LIT-

Figure 3-10. Example showing a variety of BIG ENDIAN transfers over various port sizes.

Figure 3-11. Example showing a variety of LITTLE ENDIAN transfers over various port sizes.

RULE 3.90

Figure 4-4 Advanced synchronous terminated burst

During cycle-1 the MASTER initiates a transfer. The addressed SLAVE responds in the next cycle with the assertion of ACK_O. The MASTER starts a new transfer in cycle-3. The SLAVE knows in advance it is being addressed again, therefore it keeps ACK_O asserted.

A two cycle burst now takes three cycles to complete, instead of four. This is a throughput increase of 33%. WISHBONE Classic however would require only 2 cycles. An eight cycle burst

4.1 WISHBONE Registered Feedback

WISHBONE Registered Feedback bus cycles use the Cycle Type Identifier [CTI_O()], [CT_I()] Address Tags to implement the advanced synchronous cycle termination scheme. Both MAS-

MASTER presents new address on [ADR_O()]

SETUP, EDGE 3: SLAVE decodes inputs.
SLAVE recognizes Classic Cycle and prepares response.
SLAVE prepares to send data.
MASTER monitors [ACK_I] and prepares to terminate current data phase.

CLOCK EDGE 3: SLAVE asserts [ACK_I]
SLAVE presents data on [DAT_I()].

SETUP, EDGE 4: SLAVE does not expect another transfer.
MASTER prepares to latch data on [DAT_I()].
MASTER monitors [ACK_I] and prepares to terminate current data phase.

CLOCK EDGE 4: SLAVE negates [ACK_I].
MASTER latches data on [DAT_I()]
MASTER negates [CYC_O] and [STB_O] ending the cycle

VALID

Figure 4-5 Classic Cycle

NOTE: any number of wait states can be inserted here.

SETUP, EDGE 3: MASTER is ready to transfer data again.

CLOCK, EDGE 3: MASTER presents [SEL_O].

Figure 4-7 Constant address burst

4.2.3 Incrementing Burst Cycle

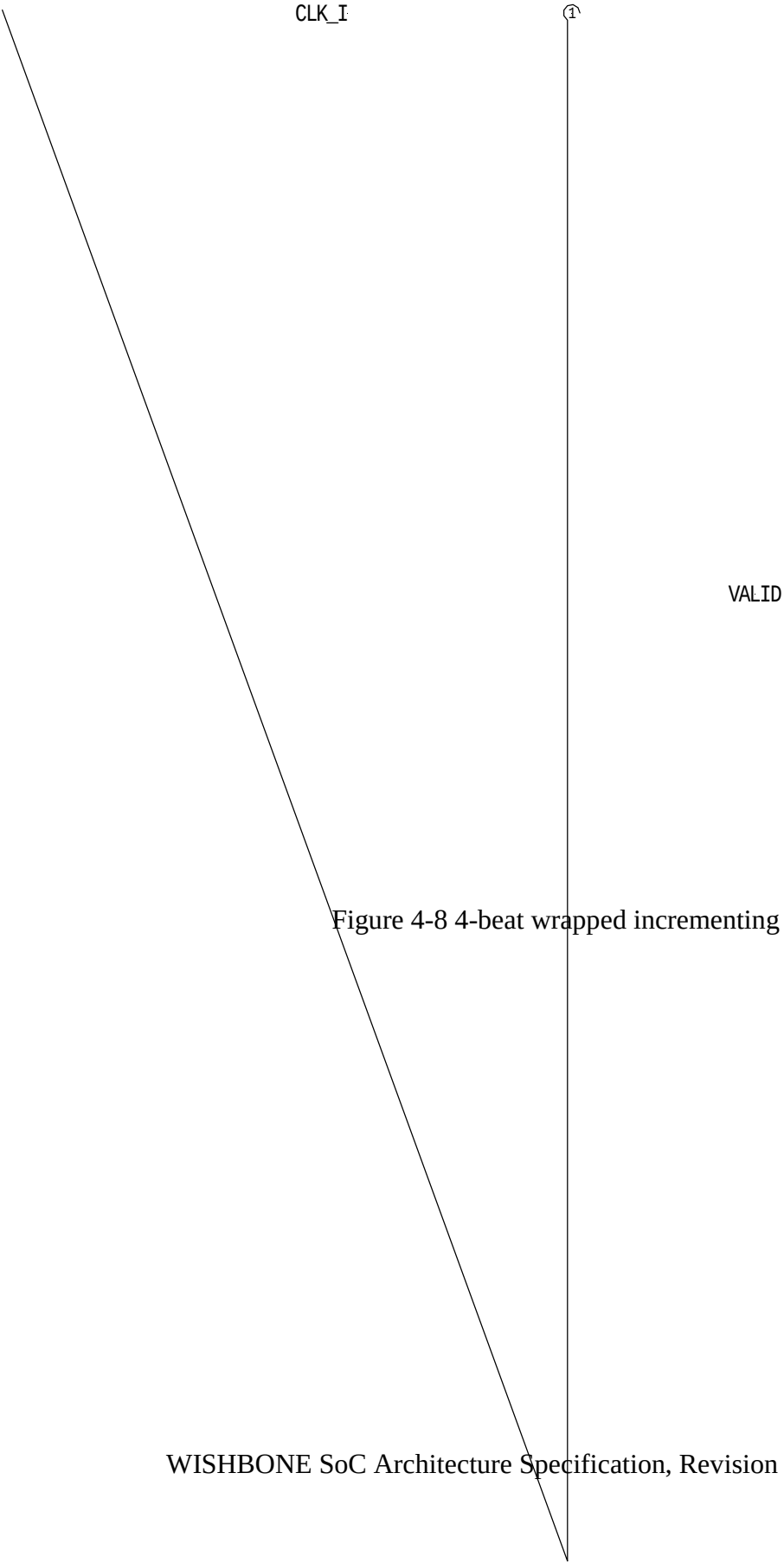

Figure 4-8 4-beat wrapped incrementing burst for a 32bit data array

Chapter 5 – Timing Specification

The WISHBONE specification is designed to provide the end user with very simple timing constraints. Although the application specific circuit(s) will vary in this regard, the interface itself is designed to work without the need for detailed timing specifications. In all cases, the only timing information that is needed by the end user is the maximum clock frequency (for [CLK_I]) that is passed to a place & route tool. The maximum clock frequency is dictated by the time delay between a positive clock edge on [CLK_I] to the setup on a stage fur1(()4.4 Tw[cf5 t– Ti thelodg iugnls pthl. T is dlac y isshpwn(ug)9.6iF[cf5 ilture5-1, a(nd is d)-10.4ecTpd,clk-su. -

SYSTEM AND METHOD FOR CAPTURING INFORMATION ON AN INTERCONNECT IN AN INTEGRATED CIRCUIT

Flynn, David W. - US Patent No. 5,525,971
INTEGRATED CIRCUIT

6.4 Methods Relating to Variable Clock Frequency

Appendix A – WISHBONE Tutorial[4]

By: Wade D. Peterson, Silicore Corporation

The WISHBONE System-on-Chip (SoC) interconnection is a method for connecting digital circuits together to form an integrated circuit ‘chip’. This tutorial provides an introduction to the WISHBONE design philosophy and its practical applications.

The WISHBONE architecture solves a very basic problem in integrated circuit design. That is, how to connect circuit functions together in a way that is simple, flexible and portable. The circuit functions are generally provided as ‘IP Cores’ (Intellectual Property Cores), which system integrators can purchase or make themselves.

Under this topology, IP Cores are the functional building blocks in the system. They are available i-11.5(y)1yyy-1ofe funcyyyrorocesstor, ser(y)-1ys ,d(y)1y i-tleo
soe pochn. Gen, mtBlogars iUndppengyrom neah othgr-72.9( )]TJT*-0.0008 Tc0.1108 Tw[and(arsat)-1(y).4(e24(

WISHBONE

Figure A-1. The WISHBONE interconnection.

The cloud analogy is used because WISHBONE can be modeled in a similar way. MASTER and SLAVE interfaces (which are analogous to the telephones) communicate thorough an interconnection (which is analogous to the telephone network 'cloud'). The WISHBONE interconnection network can be changed by the system integrator to suit his or her own needs. In WISHBONE terminology this is called a

A.2 Types of WISHBONE Interconnection

Figure A-5. Crossbar switch interconnection.

Under this method, each master arbitrates for a ‘channel’ on the switch. Once this is established, data is transferred between the MASTER and the SLAVE over a private communication link. T(e)001ii3250 cogitc10.5e SAre o10(a ppbari)-0 coblg5(an)-0 coh appcohhananeang

A.3 The WISHBONE Interface Signals

WISHBONE MASTER and SLAVE interfaces can be connected together in a number of ways.

A.4 The WISHBONE Bus Cycles

There are three types of defined WISHBONE bus cycles. They include:

- SINGLE READ/WRITE

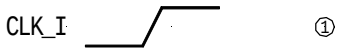

Figure A-7. SINGLE READ cycle.

A.4.2 BLOCK READ/WRITE Cycle

Now consider a system where the two processors both need to use the disk. We'll call them processor #0 and processor #1. In order for processor #0 to acquire the disk it first reads and stores the state of the semaphore bit, and then sets the bit by writing back to memory. The reading and setting of the bit takes place inside of a single RMW cycle.

Once the processor is done with the semaphore operation, it checks the state of the bit it read

A.6 SLAVE I/O Port Examples

```
entity WBOPRT16 is
port(
      -- WISHBONE SLAVE interface:
```

While most FPGA and ASIC devices will provide RAM that follows the FASM guidelines, you

Figure A-15. FASM asynchronous ROM connection and timing diagram.

Figure A-16. Simple 16 x 8-bit SLAVE memory.

Table A-4. WISHBONE DATASHEET for the 16 x 8-bit SLAVE memory.

Description	Specification

Table A-5. TAG TYPE examples.			
General Type of tag (MASTER):	Address Tag	Data Tag	Cycle Tag
Assigned TAG TYPE:			

It should be noted that the Xilinx distributed RAMs are quite efficient on the WISHBONE interface. As can be seen in the source code, only a single 'AND' gate was needed to interface the RAM to WISHBONE.

The system for the Xilinx Spartan 2 was synthesized and operated on a Silicore evaluation board. This was a 'reality check' that verified that things actually routed and worked as expected. Some

Xilinx Spartan 2 (FPGA)	XC2S50-5-PQ208C	√	53 SLICE	100 MHz	107 MHz	428 Mbyte/sec

A.10.3 Creating the Interconnection Topology

For example, consider a system with an addressing range of sixteen bits. If the addressing range were evenly split between all of the SLAVEs, then each SLAVE would be allocated 16 Kbytes of address space. This is shown in the address map of Figure A-23. In this case, the address comparator would decode bits [ADR(15..14)]. In actual practice the system integrator can alter the address map at his or her discretion.

Once a SLAVE is selected, it participates in the current bus cycle generated by the MASTER. In response to the cycle, the SLAVE must assert either its [ACK_O], [RTY_O] or [ERR_O] output. These signals are collected with an 'or' gate, and routed to the current MASTER.

Also note that during read cycles, the SLAVE places data on its [DAT_O()] bus. These are routed from the participating SLAVE to the current MASTER by way of a multiplexor. In this

Standard microcomputer buses always use the full address decoding technique. That's because the interconnection method does not allow the creation of any new signals on the interface. However, in WISHBONE this limitation does not exist. WISHBONE allows the system integrator to modify the interconnection logic and signal paths.

One advantage of the partial address decoding technique is that the size of the address decoder (on the IP core) is minimized. This speeds up the interface, as decoder logic can be relatively

Figure A-24. WISHBONE partial address decoding technique.

modules, including detailed circuit descriptions and timing diagrams. The reader is encouraged to review and experiment with all of these files.

This system was synthesized and routed on two styles of Xilinx[15] FPGA: the Spartan 2 and the

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